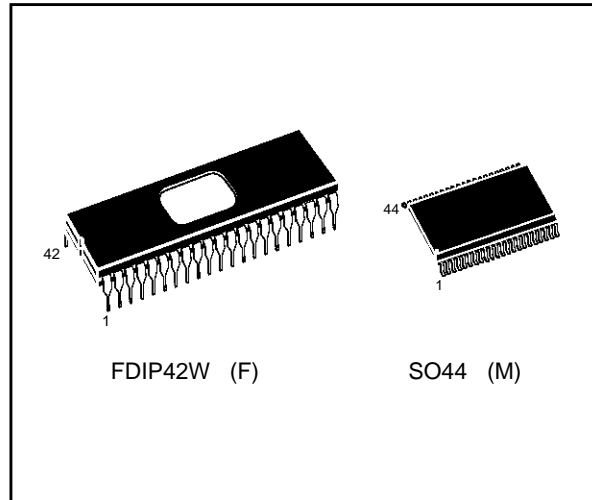


8 Megabit (1Meg x 8 or 512K x 16) UV EPROM and OTP EPROM

PRELIMINARY DATA

- FAST ACCESS TIME: 90ns
- WORD-WIDE or BYTE-WIDE CONFIGURABLE
- 8 Megabit MASK ROM COMPATIBLE
- LOW POWER CONSUMPTION
 - Active Current 70mA at 8MHz
 - Standby Current 100µA
- PROGRAMMING VOLTAGE $12.5V \pm 0.3V$
- PROGRAMMING TIME of AROUND 26sec. (PRESTO III ALGORITHM)



DESCRIPTION

The M27C800 is an 8 Megabit UV erasable and electrically programmable EPROM ideally suited for microprocessor systems requiring large data or program storage. It is organised as either 1Meg words of 8 bit or 512K words of 16 bit. The pin-out is compatible with a 8 Megabit Mask ROM.

The Window Ceramic Frit-Seal package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written rapidly to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C800 is offered in 44 pin Plastic Small Outline package.

Table 1. Signal Names

A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
Q8 - Q14	Data Outputs
Q15A-1	Data Output / Address Input
\bar{E}	Chip Enable
\bar{G}	Output Enable
$\overline{BYTEV_{PP}}$	Byte Mode / Program Supply
V _{CC}	Supply Voltage
V _{SS}	Ground

Figure 1. Logic Diagram

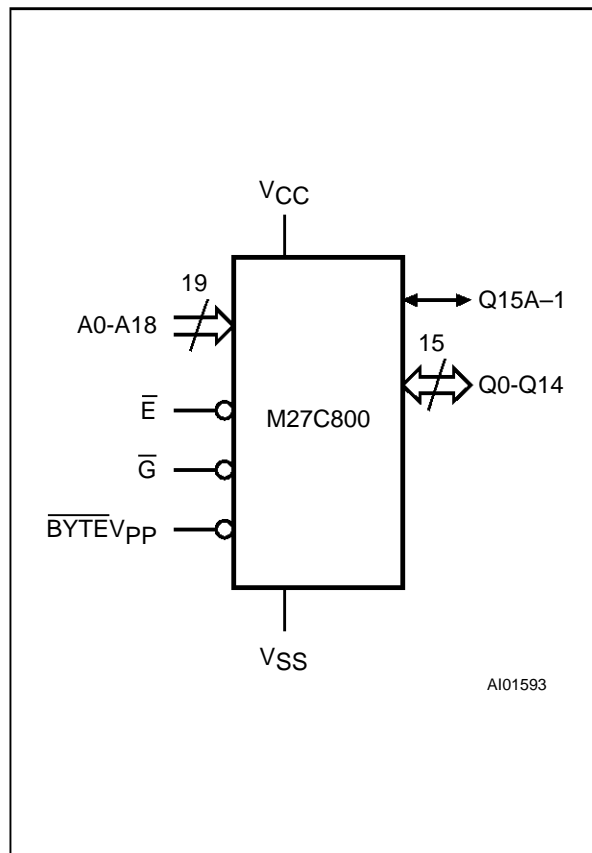
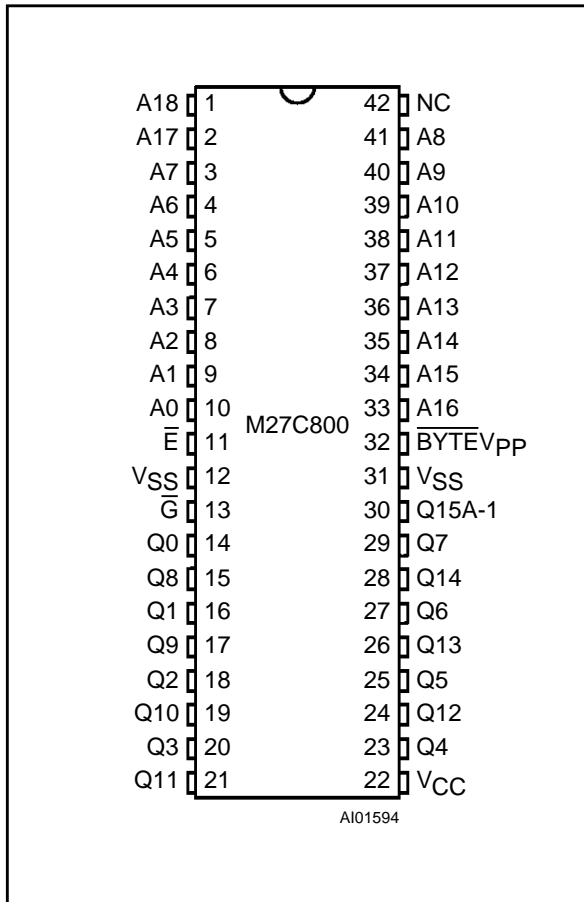
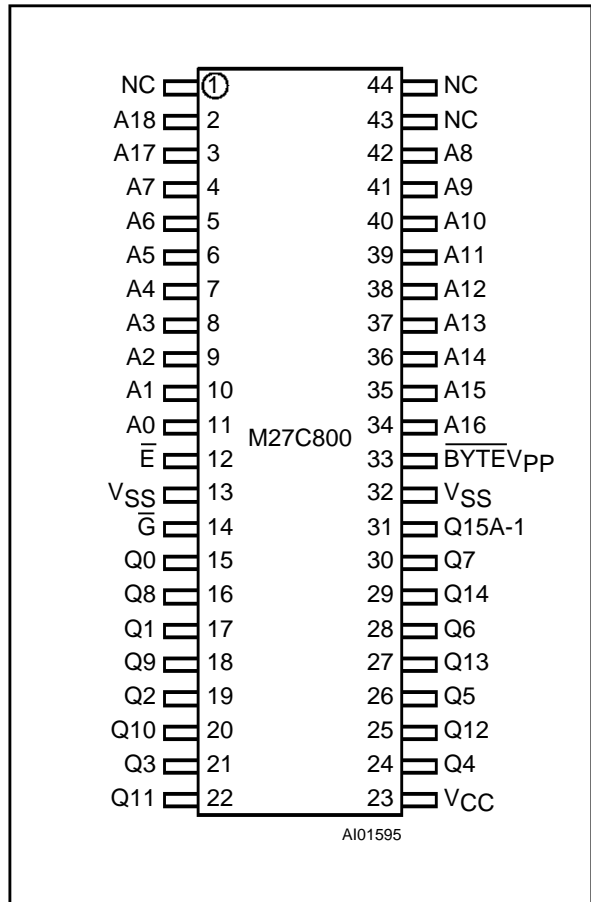


Figure 2A. DIP Pin Connections



Warning: NC = Not Connected

Figure 2B. SO Pin Connections



Warning: NC = Not Connected

Table 2. Absolute Maximum Ratings ⁽¹⁾

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature	-40 to 125	°C
T _{BIAS}	Temperature Under Bias	-50 to 125	°C
T _{STG}	Storage Temperature	-65 to 150	°C
V _{IO} ⁽²⁾	Input or Output Voltages (except A9)	-2 to 7	V
V _{CC}	Supply Voltage	-2 to 7	V
V _{A9} ⁽²⁾	A9 Voltage	-2 to 13.5	V
V _{PP}	Program Supply Voltage	-2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is -0.5V with possible undershoot to -2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	\bar{E}	\bar{G}	$\overline{BYTEV_{PP}}$	A9	Q0 - Q7	Q8 - Q14	Q15A-1
Read Word-wide	V _{IL}	V _{IL}	V _{IH}	X	Data Out	Data Out	Data Out
Read Byte-wide Upper	V _{IL}	V _{IL}	V _{IL}	X	Data Out	Hi-Z	V _{IH}
Read Byte-wide Lower	V _{IL}	V _{IL}	V _{IL}	X	Data Out	Hi-Z	V _{IL}
Output Disable	V _{IL}	V _{IH}	X	X	Hi-Z	Hi-Z	Hi-Z
Program	V _{IL} Pulse	V _{IH}	V _{PP}	X	Data In	Data In	Data In
Verify	V _{IH}	V _{IL}	V _{PP}	X	Data Out	Data Out	Data Out
Program Inhibit	V _{IH}	V _{IH}	V _{PP}	X	Hi-Z	Hi-Z	Hi-Z
Standby	V _{IH}	X	X	X	Hi-Z	Hi-Z	Hi-Z
Electronic Signature	V _{IL}	V _{IL}	V _{IH}	V _{ID}	Codes	Codes	Code

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7 or Q15	Q6 or Q14	Q5 or Q13	Q4 or Q12	Q3 or Q11	Q2 or Q10	Q1 or Q9	Q0 or Q8	Hex Data
Manufacturer's Code	V _{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V _{IH}	1	0	1	1	0	0	1	0	B2h

DEVICE OPERATION

The operating modes of the M27C800 are listed in the Operating Modes Table. A single power supply is required in the read mode. All inputs are TTL compatible except for V_{PP} and 12V on A9 for the Electronic Signature.

Read Mode

The M27C800 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the $\overline{BYTEV_{PP}}$ pin. When $\overline{BYTEV_{PP}}$ is at V_{IH} the Word-wide organisation is selected and the Q15A-1 pin is used for Q15 Data Output. When the $\overline{BYTEV_{PP}}$ pin is at V_{IL} the Byte-wide organisation is selected and the Q15A-1 pin is used for the Address Input A-1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A-1 at V_{IL} the lower 8 bits of the 16 bit data are selected and with A-1 at V_{IH} the upper 8 bits of the 16 bit data are selected.

The M27C800 has two control functions, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte-wide organisation must be selected.

Chip Enable (\bar{E}) is the power control and should be used for device selection. Output Enable (\bar{G}) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from \bar{E} to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of \bar{G} , assuming that \bar{E} has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C800 has a standby mode which reduces the active current from 50mA to 100µA. The M27C800 is placed in the standby mode by applying a CMOS high signal to the \bar{E} input. When in the standby mode, the outputs are in a high impedance state, independent of the \bar{G} input.

Table 5. AC Measurement Conditions

	High Speed	Standard
Input Rise and Fall Times	≤ 10ns	≤ 20ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

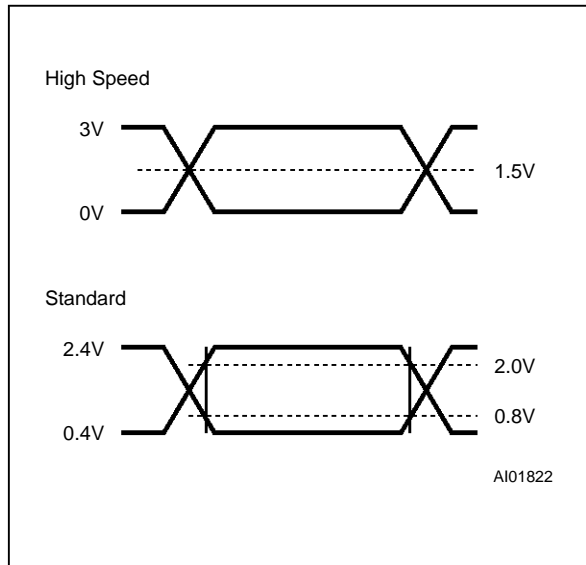


Figure 4. AC Testing Load Circuit

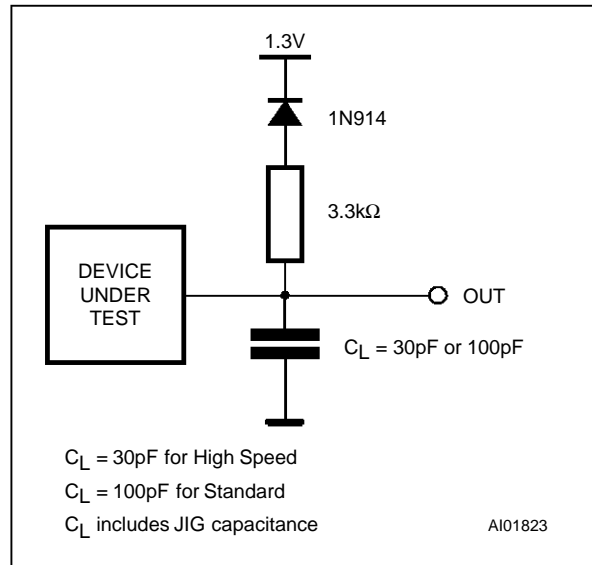


Table 6. Capacitance⁽¹⁾ (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C _{IN}	Input Capacitance (except $\overline{\text{BYTE}}V_{PP}$)	V _{IN} = 0V		10	pF
	Input Capacitance ($\overline{\text{BYTE}}V_{PP}$)	V _{IN} = 0V		120	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

- a. the lowest possible memory power dissipation,
- b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{\text{E}}$ should be decoded and used as the primary device selecting function, while $\overline{\text{G}}$ should be made a common connection to all devices in the array and connected to the $\overline{\text{READ}}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

Table 7. Read Mode DC Characteristics ⁽¹⁾
 ($T_A = 0$ to 70 °C; $V_{CC} = 5V \pm 10\%$; $V_{PP} = V_{CC}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V V_{IN} V_{CC}$		± 1	μA
I_{LO}	Output Leakage Current	$0V V_{OUT} V_{CC}$		± 10	μA
I_{CC}	Supply Current	$\bar{E} = V_{IL}, \bar{G} = V_{IL},$ $I_{OUT} = 0mA, f = 8MHz$		70	mA
I_{CC}	Supply Current	$\bar{E} = V_{IL}, \bar{G} = V_{IL},$ $I_{OUT} = 0mA, f = 5MHz$		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\bar{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\bar{E} > V_{CC} - 0.2V$		100	μA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	μA
I_{OS}	Output Short Circuit Current	Note 2 and 3		100	mA
V_{IL}	Input Low Voltage		-0.3	0.8	V
$V_{IH}^{(4)}$	Input High Voltage		2	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$		0.4	V
V_{OH}	Output High Voltage TTL	$I_{OH} = -400\mu A$	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP} .
 2. Sampled only, not 100% tested.
 3. Output shortcircuited for no more than one second. No more than one output shorted at a time.
 4. Maximum DC voltage on Output is $V_{CC} + 0.5V$.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the supplies to the devices. The supply current I_{CC} has three segments of importance to the system designer: the standby current, the active current and the transient peaks that are produced by the falling and rising edges of \bar{E} .

The magnitude of the transient current peaks is dependant on the capacitive and inductive loading of the device outputs. The associated transient voltage peaks can be suppressed by complying with

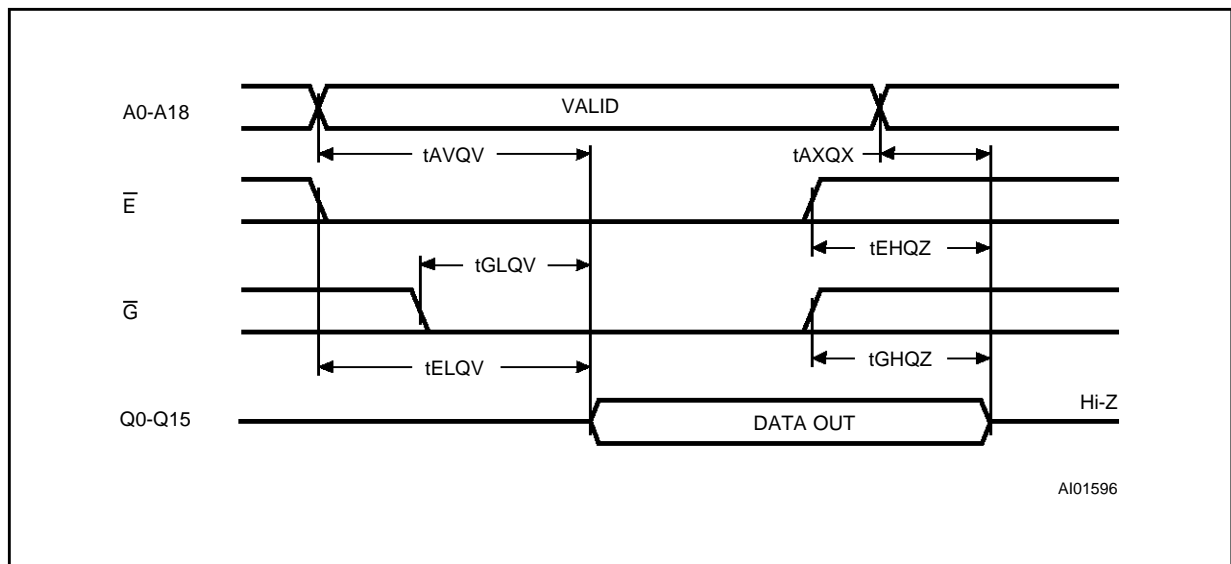
the two line output control and by properly selected decoupling capacitors. It is recommended that a $0.1\mu F$ ceramic capacitor is used on every device between V_{CC} and V_{SS} . This should be a high frequency type of low inherent inductance and should be placed as close as possible to the device. In addition, a $4.7\mu F$ electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. This capacitor should be mounted near the power supply connection point. The purpose of this capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Table 8. Read Mode AC Characteristics (1)
 (T_A = 0 to 70 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C800						Unit
				-90		-100		-120		
				Min	Max	Min	Max	Min	Max	
t _{AVQV}	t _{ACC}	Address Valid to Output Valid	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$		90		100		120	ns
t _{BHQV}	t _{ST}	BYTE High to Output Valid	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$		90		100		120	ns
t _{ELQV}	t _{CE}	Chip Enable Low to Output Valid	$\bar{G} = V_{IL}$		90		100		120	ns
t _{GLQV}	t _{OE}	Output Enable Low to Output Valid	$\bar{E} = V_{IL}$		45		50		60	ns
t _{BLQZ} (2)	t _{STD}	BYTE Low to Output Hi-Z	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$		30		40		50	ns
t _{EHQZ} (2)	t _{DF}	Chip Enable High to Output Hi-Z	$\bar{G} = V_{IL}$	0	30	0	40	0	50	ns
t _{GHQZ} (2)	t _{DF}	Output Enable High to Output Hi-Z	$\bar{E} = V_{IL}$	0	30	0	40	0	50	ns
t _{AXQX}	t _{OH}	Address Transition to Output Transition	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$	5		5		5		ns
t _{BLQX}	t _{OH}	BYTE Low to Output Transition	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$	5		5		5		ns

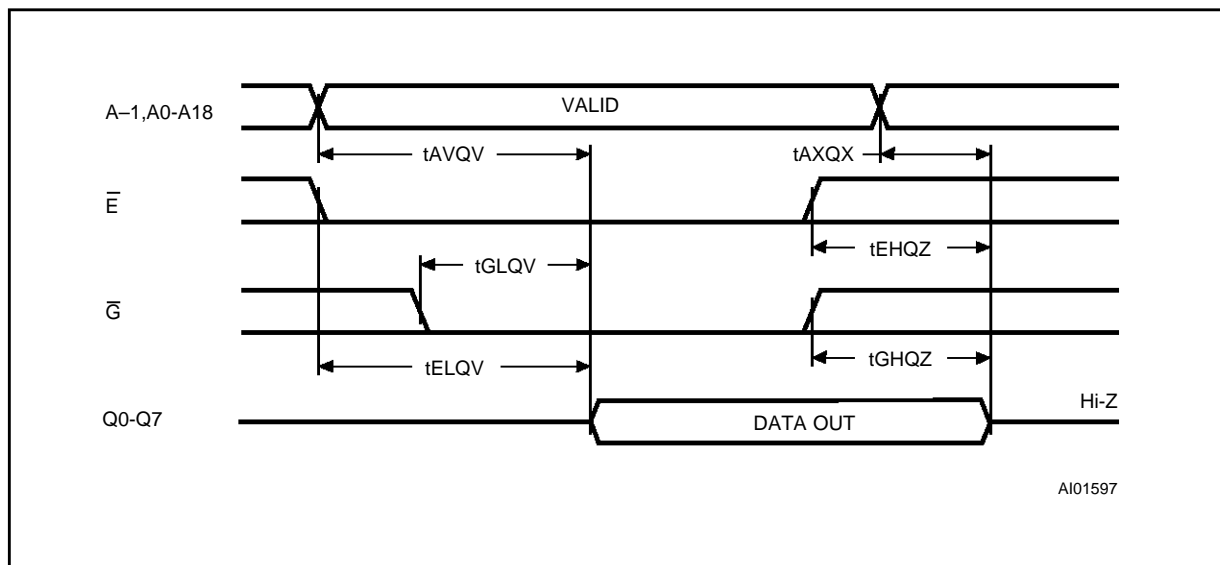
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
 2. Sampled only, not 100% tested.

Figure 5. Word-Wide Read Mode AC Waveforms



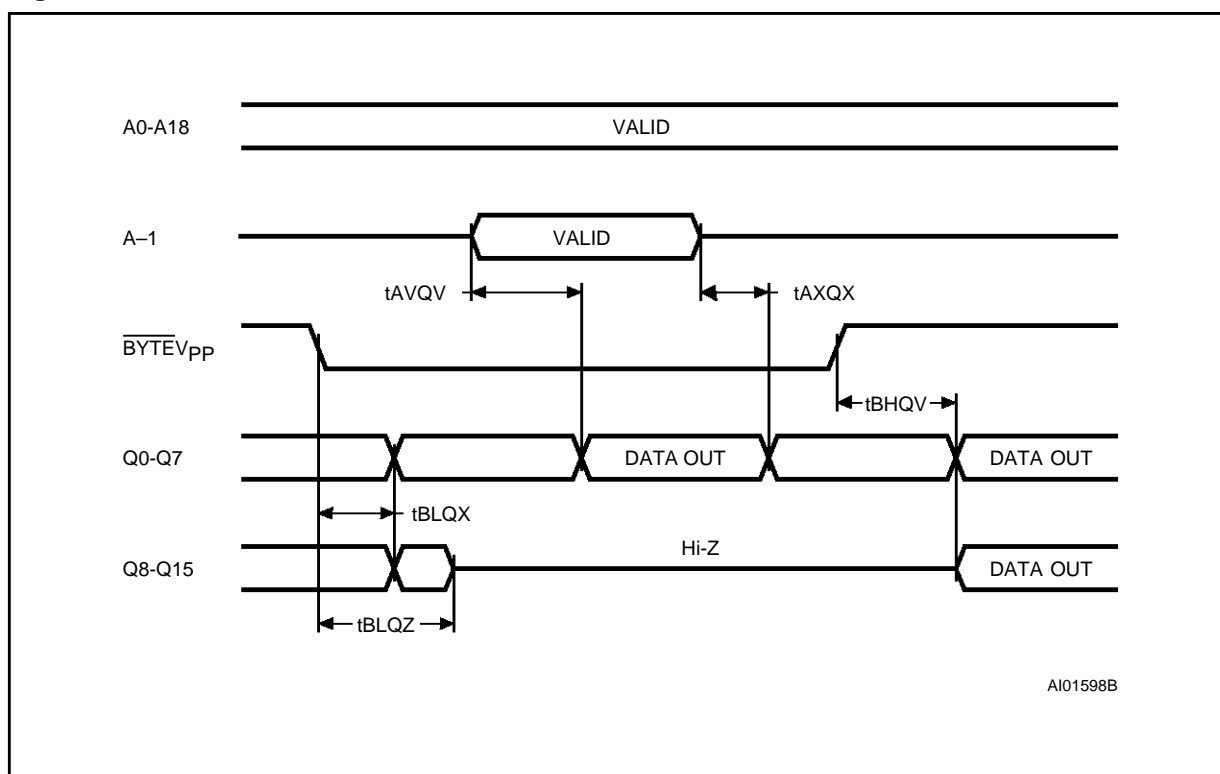
Note: $\bar{B}YTE V_{PP} = V_{IH}$

Figure 6. Byte-Wide Read Mode AC Waveforms



Note: $\overline{BYTEV}_{PP} = V_{IL}$

Figure 7. \overline{BYTE} Transition AC Waveforms



Note: \overline{E} and $\overline{G} = V_{IL}$

Table 9. Programming Mode DC Characteristics ⁽¹⁾ $(T_A = 25\text{ }^\circ\text{C}; V_{CC} = 6.25\text{V} \pm 0.25\text{V}; V_{PP} = 12.5\text{V} \pm 0.3\text{V})$

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \leq V_{IN} \leq V_{CC}$		± 1	μA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\bar{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2.4	$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$		0.4	V
V_{OH}	Output High Voltage TTL	$I_{OH} = -2.5\text{mA}$	3.5		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

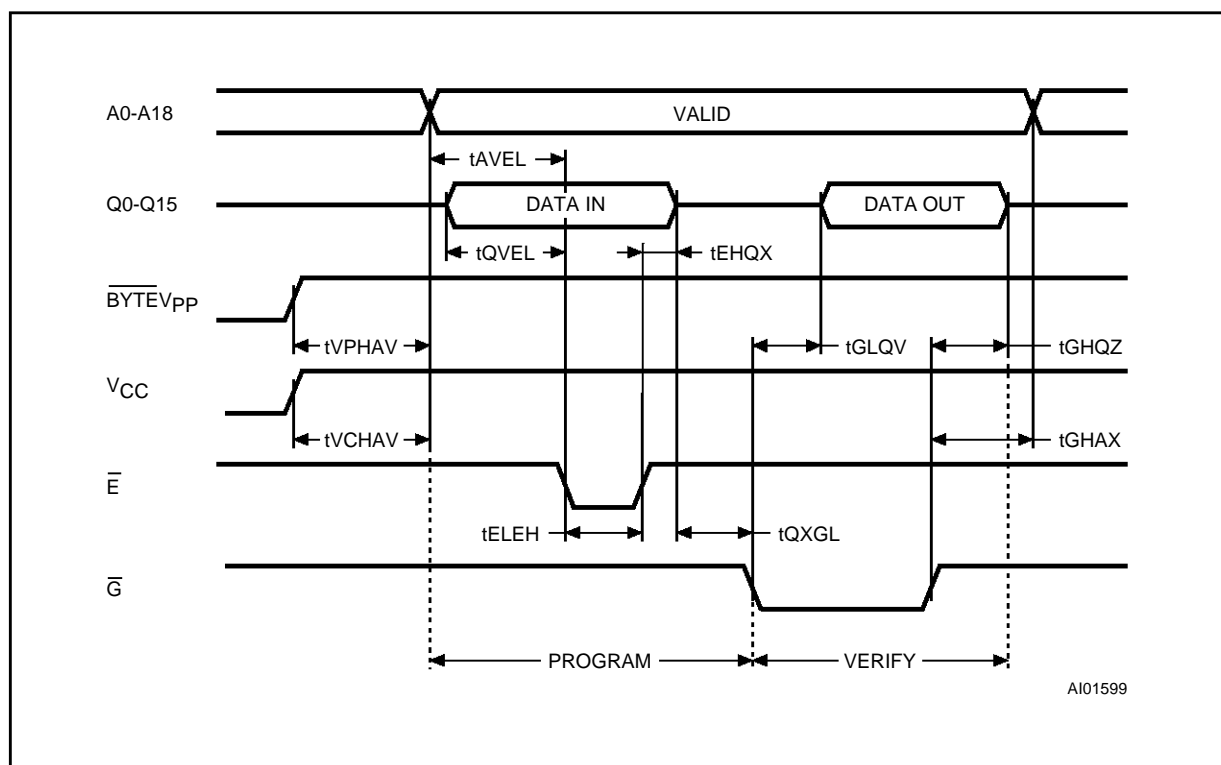
Table 10. Programming Mode AC Characteristics ⁽¹⁾ $(T_A = 25\text{ }^\circ\text{C}; V_{CC} = 6.25\text{V} \pm 0.25\text{V}; V_{PP} = 12.5\text{V} \pm 0.3\text{V})$

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		μs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		μs
t_{VPHAV}	t_{VPS}	V_{PP} High to Address Valid		2		μs
t_{VCHAV}	t_{VCS}	V_{CC} High to Address Valid		2		μs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		45	55	μs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		μs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		μs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			120	ns
$t_{GHQZ}^{(2)}$	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

2. Sampled only, not 100% tested.

Figure 8. Programming and Verify Modes AC Waveforms



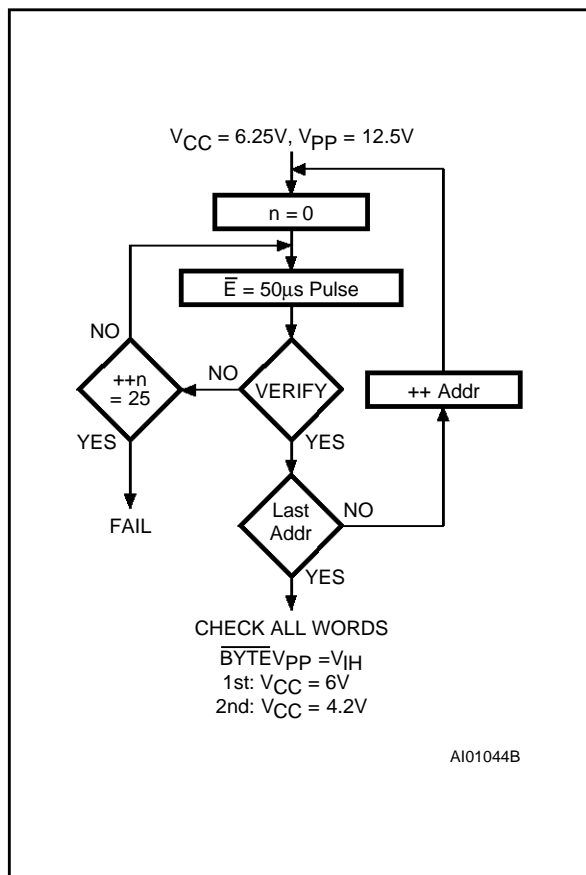
Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C800 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C800 is in the programming mode when V_{pp} input is at 12.5V, $\overline{\text{G}}$ is at V_{IH} and $\overline{\text{E}}$ is pulsed to V_{IL} . The data to be programmed is applied to 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be $6.25\text{V} \pm 0.25\text{V}$.

PRESTO III Programming Algorithm

The PRESTO III Programming Algorithm allows the whole array to be programmed with a guaranteed margin in a typical time of 26 seconds. Programming with PRESTO III consists of applying a sequence of $50\mu\text{s}$ program pulses to each word until a correct verify occurs (see Figure 9). During programming and verify operation a MARGIN MODE circuit is automatically activated to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Figure 9. Programming Flowchart



Program Inhibit

Programming of multiple M27C800s in parallel with different data is also easily accomplished. Except for \overline{E} , all like inputs including \overline{G} of the parallel M27C800 may be common. A TTL low level pulse applied to a M27C800's \overline{E} input and V_{PP} at 12.5V, will program that M27C800. A high level \overline{E} input inhibits the other M27C800s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with \overline{E} at V_{IH} and \overline{G} at V_{IL} , V_{PP} at 12.5V and V_{CC} at 6.25V.

On-Board Programming

The M27C800 can be directly programmed in the application circuit. See the relevant Application Note AN620.

Electronic Signature

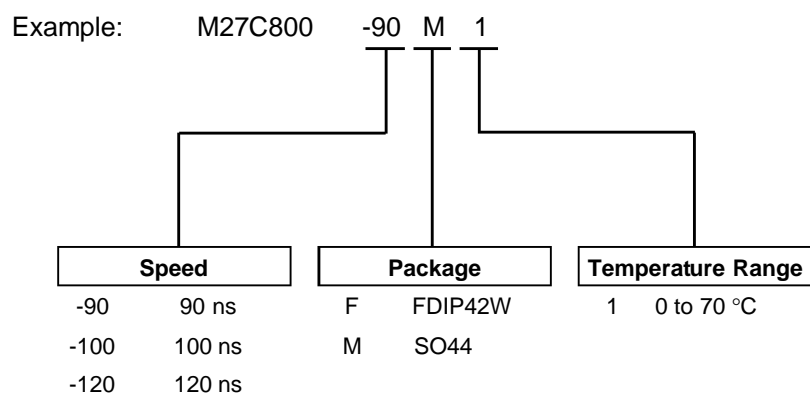
The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ambient temperature range that is required when programming the M27C800. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C800, with $V_{PP}=V_{CC}=5\text{V}$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH} . All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C800, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C800 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C800 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C800 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C800 window to prevent unintentional erasure. The recommended erasure procedure for M27C800 is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm² power rating. The M27C800 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

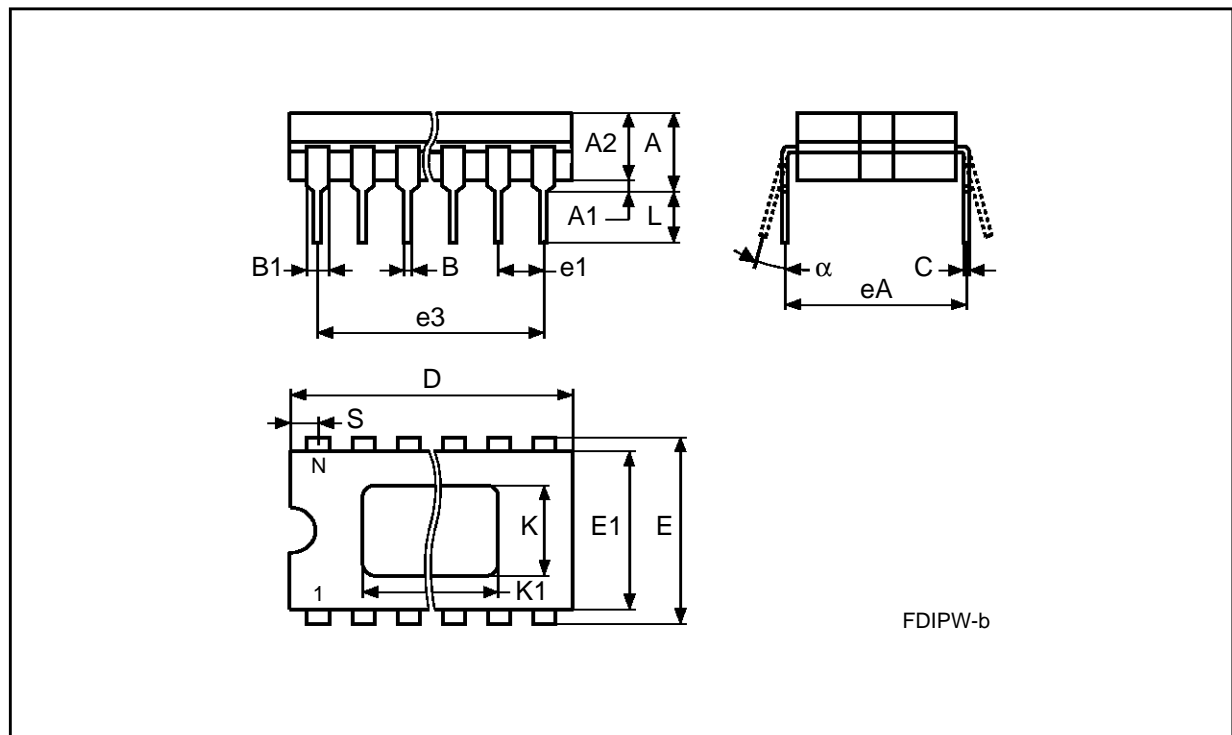


For a list of available options (Speed, Package, etc...) refer to the current Memory Shortform catalogue.
For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

FDIP42W - 42 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.27	1.52		0.050	0.060
C		0.22	0.31		0.009	0.012
D			54.81			2.158
E		15.40	15.80		0.606	0.622
E1		14.50	14.90		0.571	0.587
e1	2.54	–	–	0.100	–	–
e3	50.80	–	–	2.000	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
K		9.32	9.47		0.367	0.373
K1		11.30	11.56		0.445	0.455
α		4°	15°		4°	15°
N		42			42	

FDIP42W

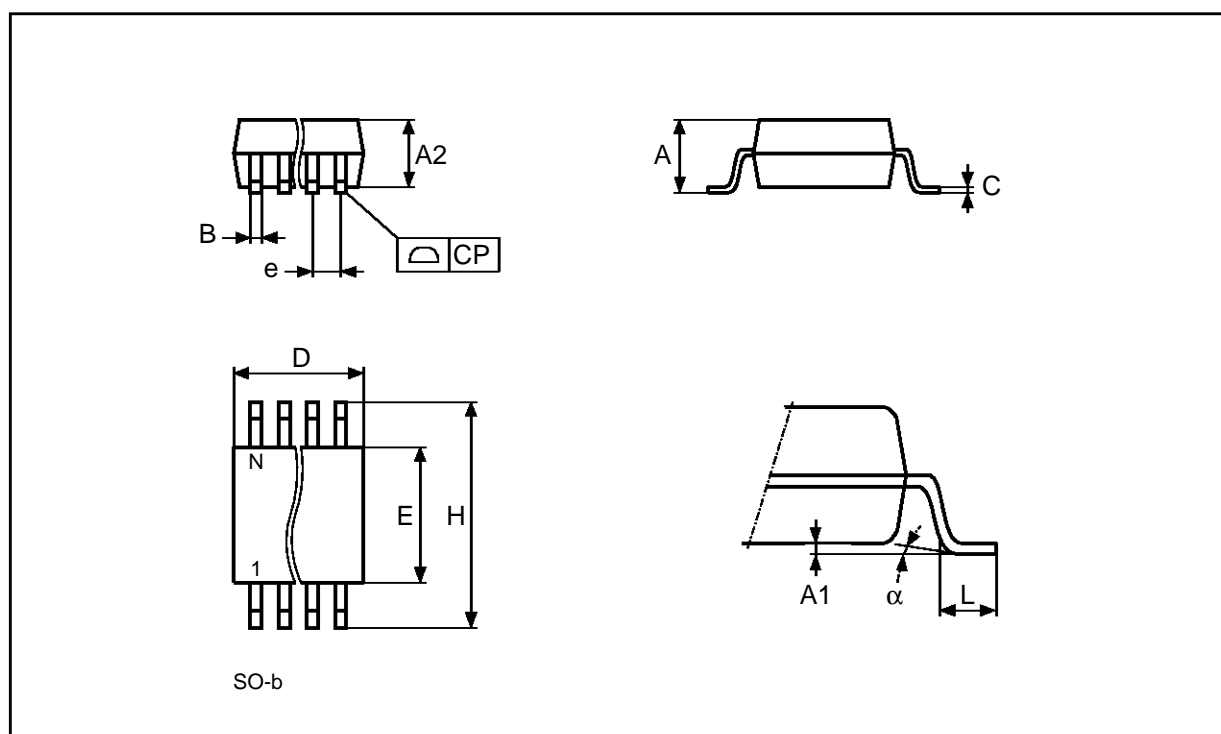


Drawing is not to scale

SO44 - 44 lead Plastic Small Outline, 525 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.42	2.62		0.095	0.103
A1		0.22	0.23		0.009	0.010
A2		2.25	2.35		0.089	0.093
B			0.50			0.020
C		0.10	0.25		0.004	0.010
D		28.10	28.30		1.106	1.114
E		13.20	13.40		0.520	0.528
e	1.27	–	–	0.050	–	–
H		15.90	16.10		0.626	0.634
L	0.80	–	–	0.031	–	–
α	3°	–	–	3°	–	–
N	44			44		
CP			0.10			0.004

SO44



Drawing is not to scale

Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1996 SGS-THOMSON Microelectronics - All Rights Reserved

SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.